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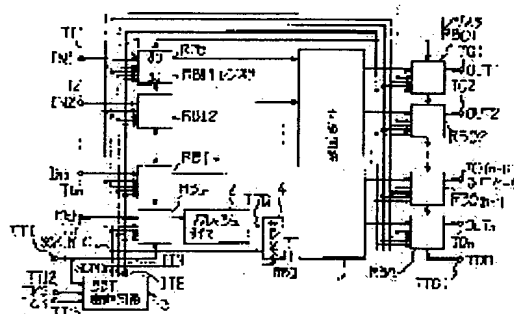
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## (54) DYNAMIC MEMORY

### (57)Abstract:

**PURPOSE:** To prevent the loss of storage data at the time of executing an internal test mode by supplying a data shifting clock as a refresh requesting signal to an internal circuit at the time of the internal test mode.

**CONSTITUTION:** When an internal test mode signal ITM is in the normal operation mode of an inactive level, a data shifting control signal SCN is also in the inactive level and a selector 4 selects a refresh requesting signal TRQ outputted by a refresh timer 2 to transfer it as a refresh requesting signal RPQ to an internal circuit 1. When the signal ITM is in the internal test mode of an active level, the selector 4 selects a data shifting clock SCK in accordance with the active level of the signal SCN to transfer it as a signal RRQ to the circuit 1. By such a constitution, the storage data in the circuit 1 are made not to be lost even when the number of signal terminals is increased and a long time is required for data shiftings.



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